AMENDMENTS

In the Claims:

Please amend the claims as indicated hereafter.

1. (Original) A method for adapting a timing loop having timing loop parameters to an environment having a broad range of frequency errors, the method comprising the steps of:

setting the timing loop parameters of the timing loop to initial values;

waiting a predetermined interval of time;

measuring a frequency error between a receiver's clock signal and a received data signal;

determining an average value of the frequency error;

subtracting the average value of the frequency error from the frequency error to produce a difference value; and

resetting the timing loop parameters to new timing loop parameter values if the difference value is less than a threshold value.

2. (Original) The method of claim 1 wherein the step of resetting the timing loop parameters to new parameter values further comprises retrieving stored timing loop parameter values from a memory.

3. (Original) The method of claim 1 further comprising the steps of replacing the threshold value with a second threshold value if the difference value is less than the threshold value and resetting the timing loop parameters to new parameter values if the difference value calculated after an interval of time is less than the second threshold value.

4. (Original) The method of claim 1 wherein the new parameter values of the timing loop parameters are less than the initial values of the timing loop parameters.

5. (Original) The method of claim 1 further comprising the steps of:

waiting a second predetermined interval of time after the difference value falls below the threshold value; and

resetting the new timing loop parameter values to a second set of new timing loop parameter values after the second predetermined interval of time has passed.

6. (Original) The method of claim 1 wherein said step of measuring a frequency error further comprises sampling a received data signal at a center sample time, an early sample time and a late sample time and calculating said frequency error based on a difference between sample values at the early sample time and the late sample time.

7. (Previously Presented) An apparatus for synchronizing a local sample clock in a receiver to a received data signal transmitted in accordance with a transmitter's clock, the apparatus comprising:

a phase error detector for producing a phase error signal wherein said phase error signal corresponds to a phase difference between said local sample clock and said received data signal;

a timing loop having timing loop parameters for receiving the phase error signal and producing a frequency error that corresponds to a frequency error between said local sample clock and said data signal; and

a processor for:

determining an average value of said frequency error between said local sample clock and said data signal;

calculating the absolute value of the difference between the frequency error and the average value of the frequency error; and

controllably adjusting the timing loop parameters to new parameter values if the absolute value of the difference between the frequency error and the average frequency error is less than a threshold value.

8. (Original) The apparatus of claim 7 wherein the processor further adjusts the timing loop parameters to a second set of new parameter values a predetermined interval of time after the difference between the frequency error and the average frequency error is less than the threshold value.

9. (Original) The apparatus of claim 7 further comprising a memory for storing the new timing loop parameter values.

10. (Original) The apparatus of claim 7 wherein the timing loop further comprises:

a first scaled path having a first gain stage wherein the first gain stage produces an output equal to the phase error signal scaled by a gain factor of α;

a second scaled path having a second gain stage wherein the second gain stage produces an output equal to the phase error signal scaled by a gain factor of β;

an accumulator coupled to the output of the second scaled path wherein the accumulator produces an output equal to an accumulated value of the output of the second gain stage; and

a summing stage for summing the output of the accumulator and the first gain stage.

11. (Original) The apparatus of claim 10 further comprising a phase accumulator for accumulating the output of the summing stage to produce a clock control output that is used to control the local sample clock in the receiver.

12. (Original) An apparatus for adaptively adjusting parameters of a timing loop to establish timing between a transmitter's clock and a receiver's clock, the apparatus comprising:

a phase error detector for detecting a phase difference between the transmitter's clock and the receiver's clock and producing an output that corresponds to the phase difference;

a first gain stage that produces an output equal to the output of the phase error detector scaled by a gain factor of α;

a second gain stage that produces an output equal to the output of the phase error detector scaled by a gain factor of β;

an accumulator for accumulating the output of the second gain stage and producing a frequency error;

a removal unit for receiving the frequency error from the accumulator and producing an output equal to the absolute value of the difference between the frequency error and an approximate average frequency error;

a threshold detector for receiving the output of the removal unit and determining if the output is less than a predetermined threshold amount; and

a gain adjuster for adjusting the gain factors α and β of the first and second gain stages to new values if the output of the removal unit is less than the predetermined threshold value.

13. (Original) The apparatus of claim 12 further comprising a memory wherein the memory stores a set of values for the gain factors α and β.

14. (Original) The apparatus of claim 13 wherein the gain adjuster further adjusts the gain factors α and β to a second set of new values a predetermined interval of time after the removal unit's output falls below the threshold value.

15. (Original) The apparatus of claim 12 wherein the removal unit further comprises a scaled path that receives the frequency error and scales the frequency error by a scaling factor, an accumulator that accumulates the scaled frequency error over a period of time, and a subtractor for removing the accumulated scaled frequency errors from the frequency error.

16. (Previously Presented) A method of adaptively adjusting timing loop parameters of a timing loop that is being utilized to synchronize a receiver's clock to a received data signal, the method comprising the steps of:

detecting a phase difference between the received data signal and the receiver's clock;

accumulating the phase difference to produce a current frequency error;

averaging the current frequency error over an interval of time to produce an average frequency error;

determining if the absolute value of the difference between the current frequency error and the average frequency error output is less than a predetermined threshold amount; and.

adjusting the timing loop parameters to new parameter values if the absolute value of the difference between the current frequency error and the average frequency error is less than the predetermined threshold value.

17. (Original) The method of claim 16 wherein the step of accumulating the phase difference to produce a current frequency error further comprises scaling the phase difference by a timing loop parameter, β, and accumulating the scaled phase difference to produce a frequency error.

18. (Original) The method of claim 17 further comprising the steps of scaling the phase difference by a timing loop parameter, α, summing the scaled phase difference with the frequency error to produce a summed output, accumulating the summed output to produce a clock control signal and using the clock control signal to modify a clock period of the receiver's clock.

19. (Original) The method of claim 18 further comprising adjusting the timing loop parameters α and β to a second set of new parameter values a predetermined interval of time after the difference between the current frequency error and the average frequency error became less than the threshold value.

20. (Original) The method of claim 19 wherein the steps of averaging the current frequency error and determining a difference between the current frequency error and the average frequency error further comprise scaling the frequency error by a gain factor, accumulating the scaled frequency errors and subtracting the accumulated scaled frequency errors from the current frequency error.

21-22. (Canceled)

23. (Currently Amended) ~~The method of claim 22, further~~ A method for adaptively adjusting parameters of a timing loop, the method comprising the steps of:

measuring a frequency error of a clock signal of a receiver;

determining a value indicative of an average of the frequency error over time;

adaptively adjusting, based on the value, parameters of a timing loop of the receiver;

combining the value with a value indicative of a current frequency error of the clock signal, thereby providing a combined value; and

comparing the combined value to a threshold,

wherein the adjusting step is based on the comparing step.

24. (Previously Presented) The method of claim 23, wherein the combined value is indicative of a difference between the average and the current frequency error.